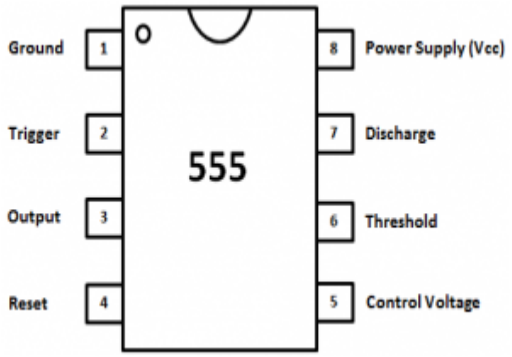
Model test paper

Sub-Linear Integrated Electronic Circuit

EL-307

Q.1 Draw and explain Pin diagram of 555 Timer circuit?

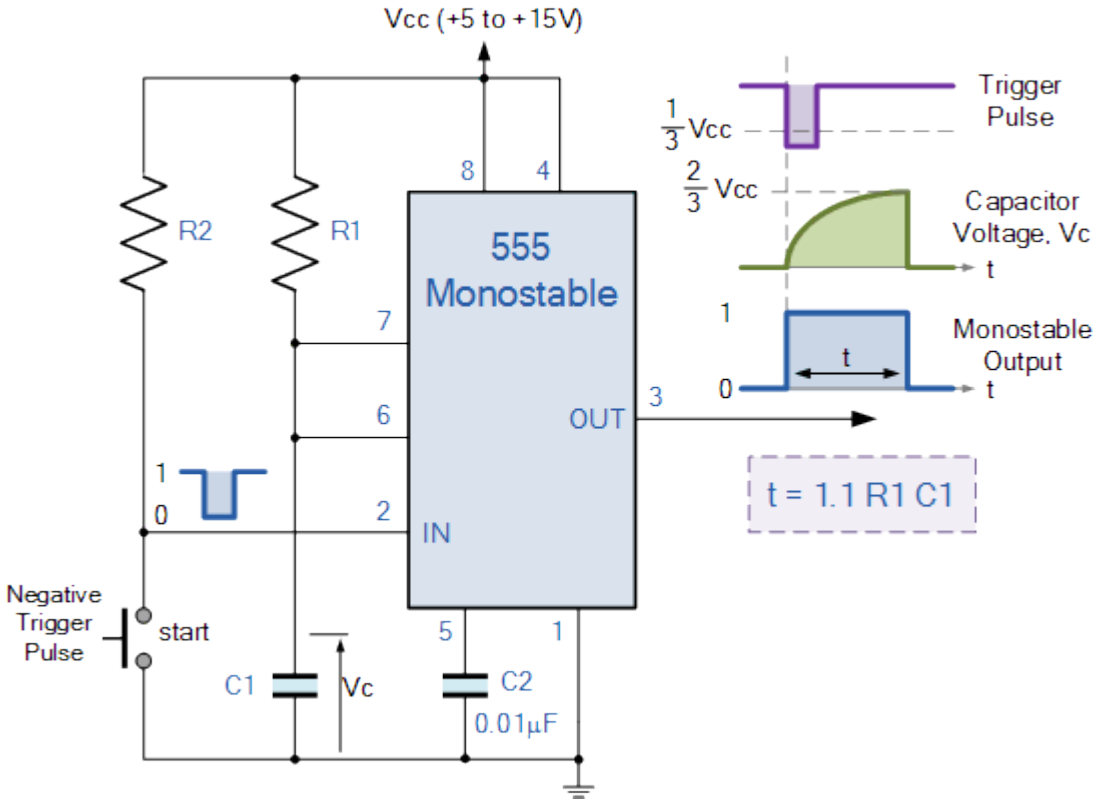


Pin diagram and description

Pin	Name	Purpose
1	GND	Ground reference voltage, low level (0 V)
2	TRIG	The OUT pin goes high and a timing interval starts when this input falls below 1/2 of CTRL voltage (which is typically 1/3 *V*cc, CTRL being 2/3 *V*cc by default if CTRL is left open). In other words, OUT is high as long as the trigger low. Output of the timer totally depends upon the amplitude of the external trigger voltage applied to this pin.
3	OUT	This output is driven to approximately 1.7 V below +*V*cc, or to GND.
4	RESET	A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Overrides TRIG which overrides threshold.
5	CTRL	Provides "control" access to the internal voltage divider (by default, 2/3 *V*cc).
6	THR	The timing (OUT high) interval ends when the voltage at threshold is greater than that at CTRL (2/3 *V*cc if CTRL is open).

7	DIS	Open collector output which may discharge a capacitor between intervals. In phase with output.
8	*V*cc	Positive supply voltage, which is usually between 3 and 15 V depending on the variation.

Q.2 Explain 555 timer as a astable multivibrator?



When a negative (0V) pulse is applied to the trigger input (pin 2) of the Monostable configured 555 Timer oscillator, the internal comparator, (comparator No1) detects this input and "sets" the state of the flip-flop, changing the output from a "LOW" state to a "HIGH" state. This action in turn turns "OFF" the discharge transistor connected to pin 7, thereby removing the short circuit across the external timing capacitor, C1.

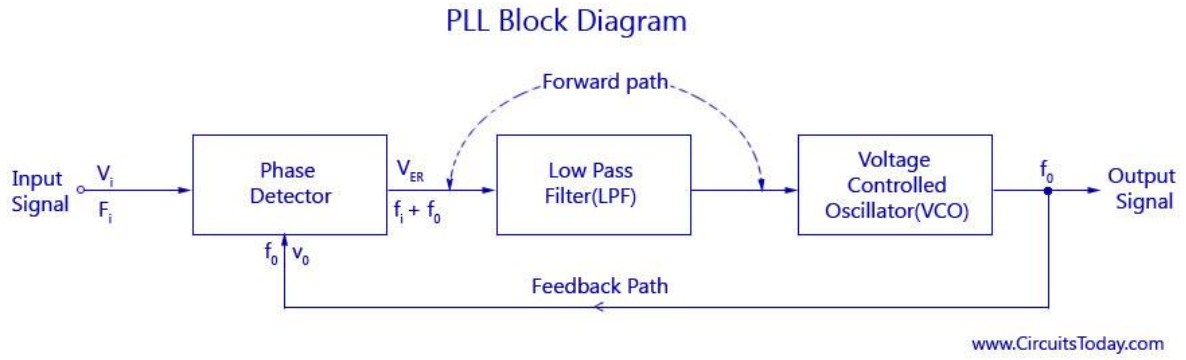
This action allows the timing capacitor to start to charge up through resistor, R1 until the voltage across the capacitor reaches the threshold (pin 6) voltage of 2/3Vcc set up by the internal voltage divider network. At this point the comparators output goes "HIGH" and "resets" the flip-flop back to its original state which in turn turns "ON" the transistor and discharges the capacitor to ground through pin 7. This causes the output to change its state back to the original stable "LOW" value awaiting another trigger pulse to start the timing process over again. Then as before, the Monostable Multivibrator has only "ONE" stable state.

The **Monostable 555 Timer** circuit triggers on a negative-going pulse applied to pin 2 and this trigger pulse must be much shorter than the output pulse width allowing time for the timing capacitor to charge and then discharge fully. Once triggered, the 555 Monostable will remain in this "HIGH" unstable output state until the time period set up by the R_1 x C_1network has elapsed. The amount of time that the output voltage remains "HIGH" or at a logic "1" level, is given by the following time constant equation.

$$\tau = 1.1 R_1 C_1$$

Where, t is in seconds, R is in Ω and C in Farads.

Q.3 Draw and Explain block diagram of PLL?



The block diagram of a basic PLL is shown in the figure below. It is basically a flip flop consisting of a phase detector, a low pass filter (LPF),and a Voltage Controlled Oscillator (VCO).

The input signal Vi with an input frequency fi is passed through a phase detector. A phase detector basically a comparator which compares the input frequency fiwith the feedback frequency fo .The phase detector provides an output error voltage Ver (=fi+fo),which is a DC voltage. This DC voltage is then passed on to an LPF. The LPF removes the high frequency noise and produces a steady DC level, Vf (=Fi-Fo). Vf also represents the dynamic characteristics of the PLL.

The DC level is then passed on to a VCO. The output frequency of the VCO (fo) is directly proportional to the input signal. Both the input frequency and output frequency are compared and adjusted through feedback loops until the output frequency equals the input frequency. Thus the PLL works in these stages – free-running, capture and phase lock.

As the name suggests, the free running stage refer to the stage when there is no input voltage applied. As soon as the input frequency is applied the VCO starts to change and begin producing an output frequency for comparison this stage is called the capture stage. The frequency comparison stops as soon as the output frequency is adjusted to become equal to the input frequency. This stage is called the phase locked state.

Now let us study in detail about the various parts of a PLL – The phase detector, Low Pass Filter and Voltage Controlled Oscillator.