

# MODEL TEST PAPER

SUB CODE EE301 / EL 305

EE-III year

Q.1: SCR & TRIAC are respectively

- (A) Both are unidirectional
- (B) Both are bidirectional
- (C) SCR is unidirectional & TRIAC are bidirectional
- (D) SCR is bidirectional & TRIAC is unidirectional

[C]

Q.2: what is holding current & latching current?

→ Holding current: - minimum value of current that must be there to provide a path between anode & cathode to flow anode current to maintain SCR in on state. Below holding current SCR will be off.

Latching current: - min Anode current required to maintain a thyristor in on state immediately after SCR is triggered on. Its value is greater than latching current.

Q.3 what is the difference between ~~SCR~~ SCR & TRIAC?

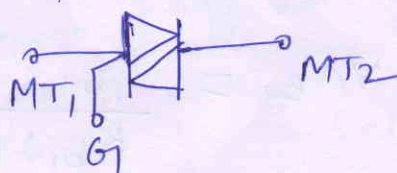
SCR

① symbol



TRIAC

symbol



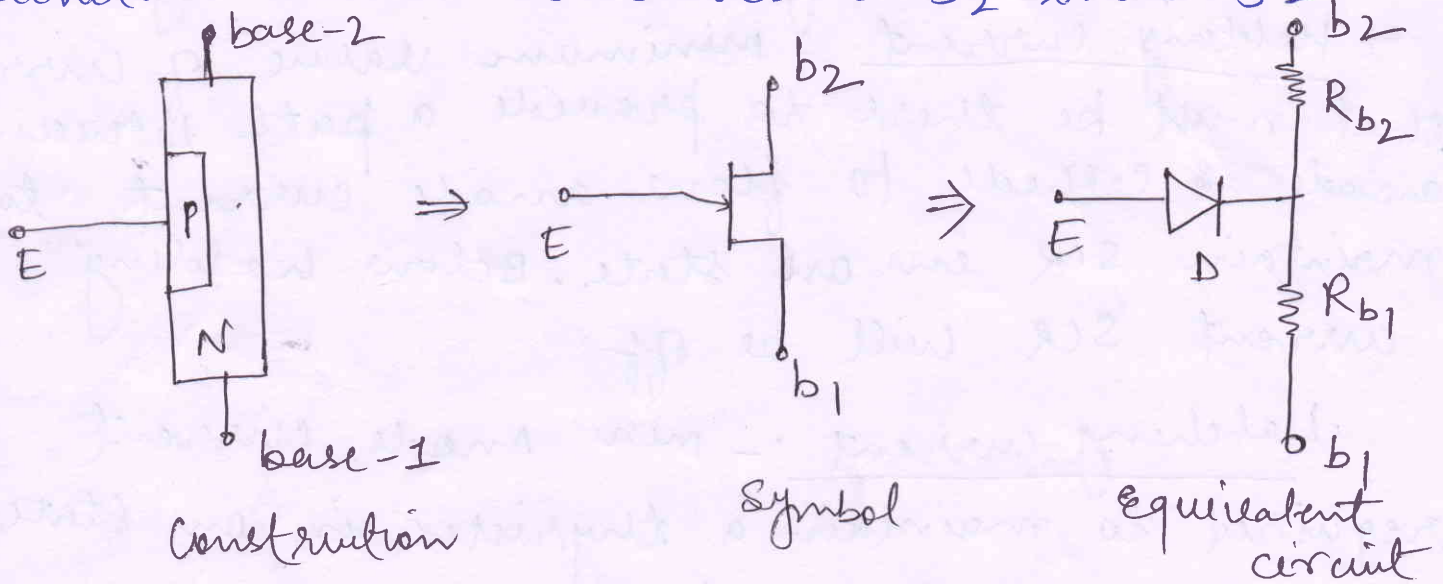
2) Available in Large ratings

Available in Smaller ratings

- 3) SCR can be triggered by positive gate volt only. | Triac can be triggered either by positive or negative gate voltage
- 4) It control DC power | Control DC as well as AC power.

Q.3 : Explain UJT construction, operation & application?

Ans:- UJT refers to unijunction transistor. It has 3 terminals emitter & two bases. i.e. E, B<sub>1</sub>, B<sub>2</sub>. The base is formed by a lightly doped n-type bar of silicon. Emitter is of p-type heavily doped junction. Emitter is closer to B<sub>2</sub> than B<sub>1</sub>.



It is called unijunction transistor because there is single junction formed by embedding in of n-type Si base & p-type emitter.

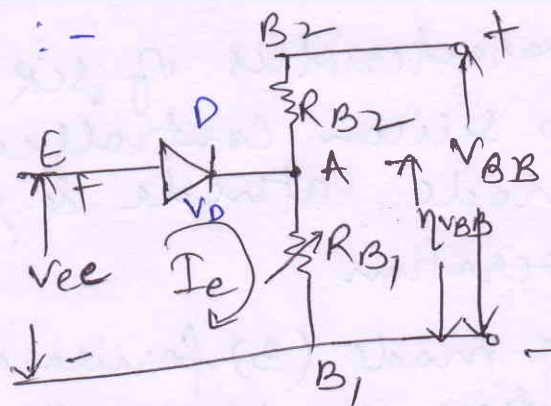
When a volt  $V_{BB}$  is applied across the two base terminals B<sub>1</sub> & B<sub>2</sub>; potential of point A w.r.t B<sub>1</sub> is given by

$$V_{AB_1} = \frac{R_{b1} \cdot V_{BB}}{R_{b1} + R_{b2}} = \eta \cdot V_{BB}$$

$$\eta = \frac{R_{b1}}{R_{b1} + R_{b2}} \rightarrow \text{Intrinsic stand off ratio} \rightarrow 0.5 - 0.8$$



## UJT operation :-



When volt  $V_{BB}$  is applied between base  $b_1$  &  $b_2$  than volt  $V_A = nV_{BB}$  & this volt acts as  $R_B$  on diode  $D$ . if  $V_{EE} < V_A$  there is no current flow in emitter due to Reverse biasing of diode. if  $V_{EE} \geq nV_{BB} + V_D$  than current flow through diode  $D$ .

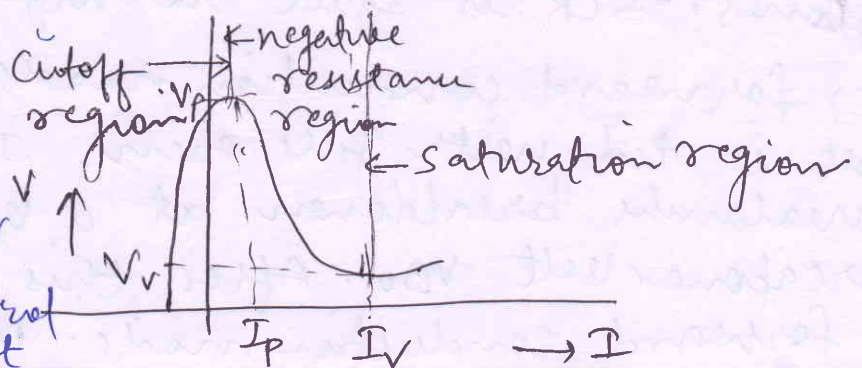
There are 3 regions in UJT

1. Cutoff region - No current flow in emitter circuit and UJT is off in this state.
2. Negative resistance region - emitter volt. is decreased to valley point volt and emitter current is increased. due to flow of current in  $b_1$ , no of  $e^-$  is increased so resistance  $R_{B1}$  is decreased. since  $R_{B1}$   $\downarrow$  as volt  $\uparrow$  hence it is called negative resistance region. Flow of current into UJT emitter causes resistive value of  $R_{B1}$  to  $\downarrow$ , allowing more current flow.

(3) Saturation Region: - Increasing VEE keeps emitter voltage constant but emitter current increases

## Application :-

- (1) used as a relaxation oscillator
- (2) used in phase control circuit





Q:4 Explain V-I characteristics of SCR with graph?

Ans: - SCR refers to Silicon Controlled Rectifier. It has 3 terminals Anode, Cathode & gate. It has 3 basic modes of operation

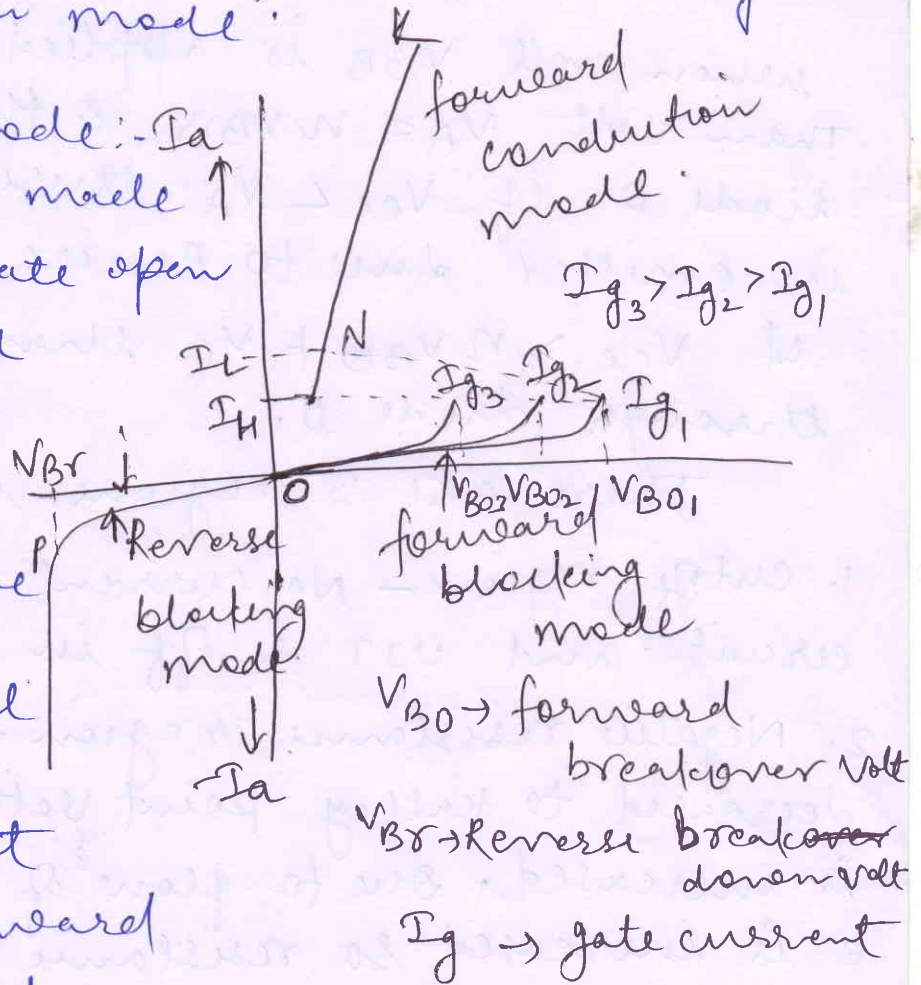
(A) Reverse Blocking mode (B) forward blocking mode (C) forward conduction mode.

(A) Reverse blocking mode: -  $I_a$  when cathode is made +ve w.r.t Anode & gate open & SCR is Reverse biased and small current of few mA will flow. This is R.B mode.

⊙ P. if reverse volt is tied to breakdown level  $V_{BR}$ , an avalanche breakdown occurs at  $J_1$  &  $J_3$ .  $J_2$  is forward biased. In this mode device offers high impedance state.

(B) forward Blocking mode → when Anode is positive w.r.t cathode, & gate open. SCR is forward biased.  $J_1, J_3$  is forward biased and  $J_2$  is R.B. in this mode small forward leakage current flows. SCR is still in high impedance state.

(C) forward conduction mode: - when A-K forward volt is tied with gate open,  $J_2$  will have an avalanche breakdown at a volt called forward breakdown volt  $V_{BO}$ . After this SCR entered into forward conduction mode. NK.



$V_{BO}$  → forward breakdown volt  
 $V_{BR}$  → Reverse breakdown volt  
 $I_g$  → gate current