Q.1 Operator किसे कहते हैं? यह कितने प्रकार के होते हैं? एक त्रिभुज का क्षेत्रफल ज्ञात करने के लिए प्रोग्राम लिखिये जबकि त्रिभुज की तीनों भुजायें a, b, c ज्ञात हों?

Ans:- Operator → कम्प्युटर द्वारा गणनायें कराने के लिए प्रोग्राम में कुछ प्रतीकों (Symbols) का उपयोग किया जाता है। इन प्रतीकों को Operator कहा जाता है।

संकारक 7 प्रकार के होते हैं।

1. अंकगणितीय संकारक (Arithmetic Operators)
2. तुलनात्मक संकारक (Relational Operators)
3. तार्किक संकारक (Logical Operators)
4. एकल संकारक (unary Operators)
5. निर्धारण संकारक (Assignment Operators)
6. कन्डीशनल संकारक (conditional Operators)
7. बिटवाइज संकारक (Bit wise Operators)

Program:- Formula $\sqrt{S(S-a)(S-b)(S-c)}$ where $S=(a+b+c)/2$

```
#include<stdio.h>
#include<conio.h>
#include<math.h>
void main()
{
  float a,b,c, area;
Printf("Enter the value of a,b and c\n");
Scanf("%f%f%f &a, &b, &c); S=(a+b+c)/2;
Printf("The area of the Triangle is: %f',area);
  getch();
}
```

Result:- Enter the value of a, b and c :- 5 5 5

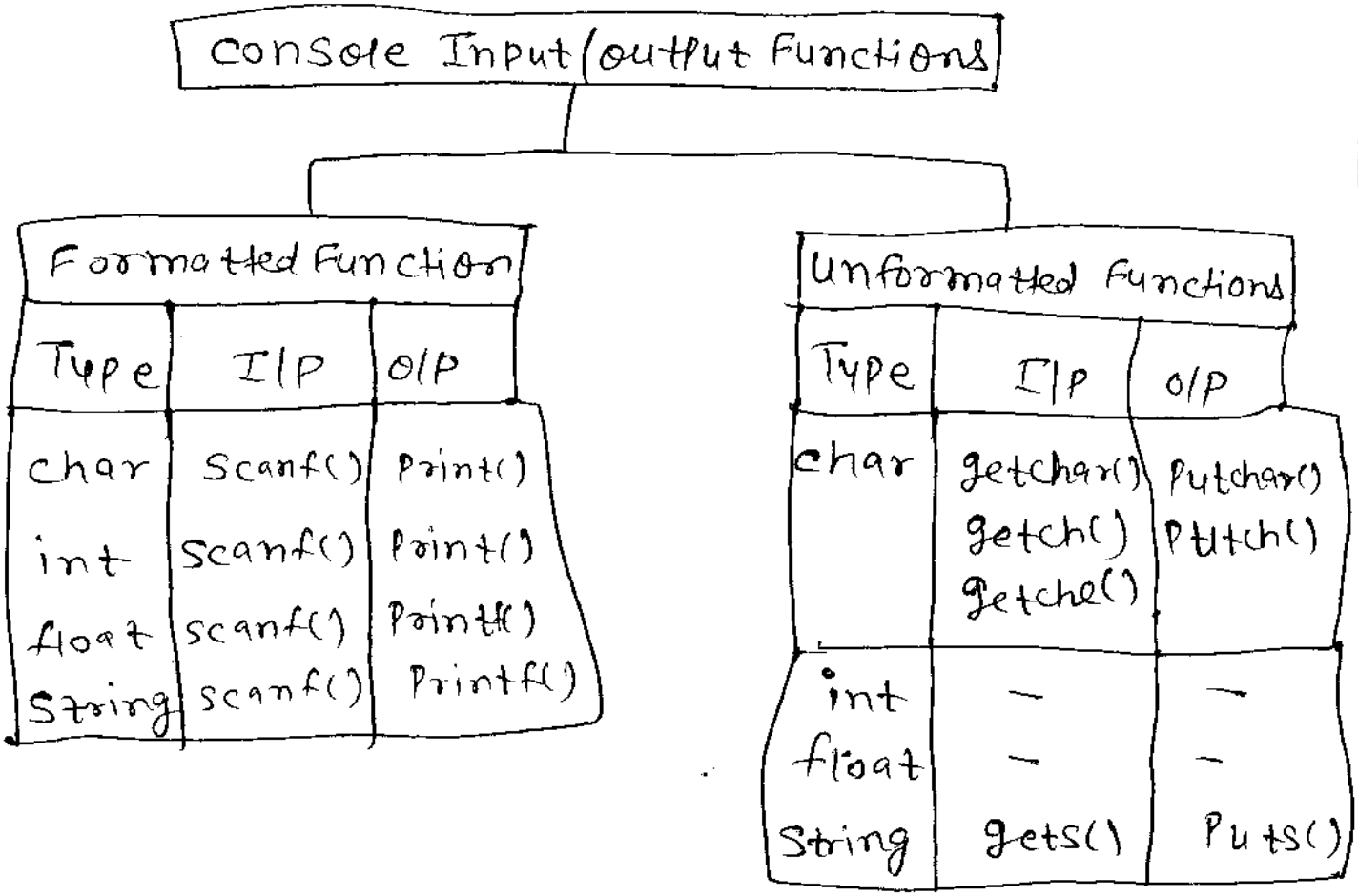
The area of the triangle is:- 10.825317

nsole I/P & O/P फलनों को समझाइए?

- Console Input/output → console इनपुट आउटपुट को दो वर्गों में बाँटा गया है।(दो भाग)

1. Unformatted console Input/output functions
2. Formatted console Input/output functions

इन दोनो में मुख्य अन्तर यह है कि फॉरमेटेड कन्सोल I/P & O/P फलन की बोर्ड से डाटा लेता है तथा आउटपुट VDU पर डाटा user की आवश्यकता के अनुसार Formatted रुप में भेजता है जबकि unformatted में एक ही प्रकार से data प्राप्त कर सकते है। जैसे हमे Total item तथा sale item को VDU पर प्रिन्ट करना है तो वह VDU पर कहाँ पर Print होगा तथा इनके मध्य कितनी जगह होगी यह हम केवल Formatted console Input/output के द्वारा ही कर सकते है।



Q.3 control statement को समझाइए? ये कितने प्रकार के होते हैं? दो संख्याओं की तुलना करने हेतु if कथन का प्रयोग करते हुऐ Program लिखिए?

Ans:- control statement → कथनो का निष्पादन उस क्रम में होता है जिस क्रम में वो लिखे हुए होते है और कथन एक बार ही निष्पादित होता है।

gram साधारण Program होता है। परन्तु बहुत Program में तार्किक (Logical statement) लिखने की आवश्यकता होती है जो कि कथनों के निष्पादन का क्रम तय करते है। इसमें condition के सही (True) होने पर कथनों का निष्पादन होता है। तथा गलत (False) होने पर अलग कथनों का निष्पादन करते है।

Control statement 3 प्रकार के होते हैं।

1. निर्णय करने वाले कथन (Decision making statement)
   (i) if statement
   (ii) if else statement
   (iii) switch statement
2. लूप बनाने वाले कथन (LOOP statements)
   (i) For LOOP
   (ii) while LOOP
   (iii) do-while LOOP
3. अन्य नियंत्रण कथन (other control statements)
   (i) Break
   (ii) continue
   (iii) go to
   (iv) exit

Program:-
```
#include <stdio.h>
#include <conio.h>
main()
{
  int x;
  clrscr();
  x = 10;
  if (x>5)
 Printf("x is greater than 5");
  getch();
}
```

Output:- x is greater than 5

Q. 4 what is an array? Explain with example?

ऐरे एक ऐसा चर होता है। जो समान विशेषताओं वाले आँकड़ो (data) के समूह को स्टोर कर सकता है। इसमे समूह के प्रत्येक आँकड़े (data) को उसके सूचकांक (Index) द्वारा उल्लेख करते है। आँकड़ो का प्रकार int, float, char या double हो सकता है।

Example → यदि किसी class में 20 Student हो तो उनके अंको को भंडारित करने के लिए marks नामक array का उपयोग कर सकते है, जिसे marks(20) के नाम से जानेंगे। 20 यह बताता है कि, marks कुल 20 आँकड़े का समूह है। प्रत्येक आँकड़े की स्थिति को सूचकांक (Index) के द्वारा पहचाना जाता है।

Model Question Paper

CS-203

Q-1 What is deadlock. What are necessary conditions for deadlock.

Ans. Deadlock – In Multiprogramming environment as several Processes compete for the finite no. of resources, the Process request for resources, if they are available the Process get them otherwise they have to go to waiting state. The waiting state of the Process may not change if the requested resource is unavailable and if such waiting Processes hold some resources and they will not release them till their execution Completion. A hanging situation in the system may result in such situation, and this situation is called a deadlock.

There are four conditions that must be simultaneously true for deadlock to occur.

i) Hold and wait – The Process to be deadlocked must hold an instance of resource of many instances of a resource and wait for instances of other resources that are held by other Processes.

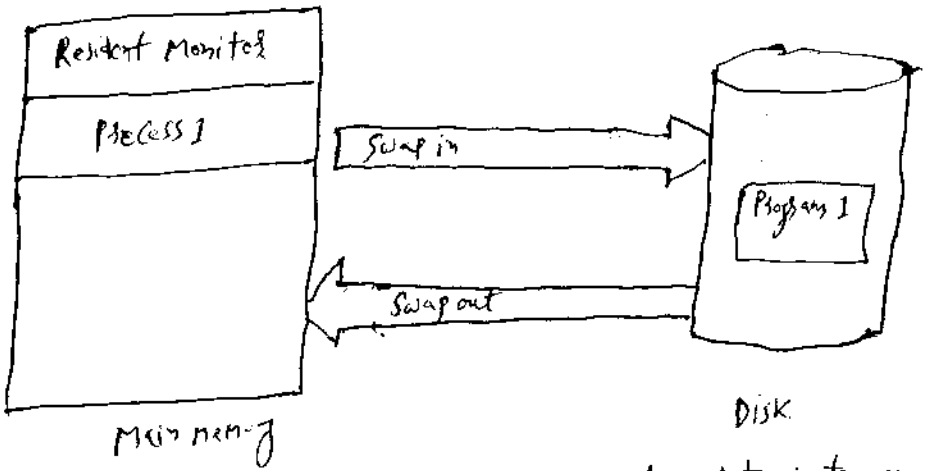
ii) No Sharing of resources – most of the resources in the system are non-shareable in nature. It means that once the instance of a resource is allocated to a process, other process can not use that instance.

iii) No Preemption – once the instance of instances of a resource is allocated to a Process. then they are not Preempted by the system until the Process release them voluntarily. It is called no-Preemption.

iv) Circular wait – A waiting for the Instance of resource by the Process must be Circular. Means if there are n Processes and if we start from Process P1, then P1 must wait for the instance held by P2. P2 must wait for the instance held by P3 and so on, so P(n-1) must wait for an instance held by Pn and Pn must wait for an instance held by P1. If there is no Circular wait then there is no deadlock in the system.

2 What is swapping. Explain with example.

Ans.



The Program that is ready for execution must be brought into main memory for execution. Then the passive Program when it is brought into main memory becomes active for execution and is termed as Process. In CPU Scheduling that there must be always some Process residing in main memory for execution, to improve the Performance of CPU. In Case of Preemptive scheduling the executing Process may be Preempted so that to allocate Processor to other Processes. The later Process must be brought into main memory from the disk (Secondary Storage). The former Process may be ~~take~~ take back into disk (Secondary Storage) from memory so that to accomodate the later Process. This Procedure of Operating System memory manager to move the Process ~~from~~ to the disk from memory and to the memory from the disk is called as Swapping. When the Process is moved from memory to the disk, the Procedure is swapped-out and when the Program is brought into main memory from disk, then the Procedure is called swap-in. The ~~to~~ swapping of Processes increases turn around time.

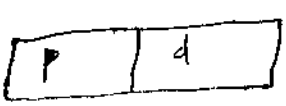
3 What is Paging. Explain the concept of Paging.

Ans. Paging – This is the memory management scheme in which the User Programs need not be stored in main memory contiguously. The parts of the Programs may be scattered in the memory. So this scheme of memory management is called non-contiguous memory management.

The implementation of no-contiguity is done by means of dividing the 'logical memory' User Programs into equal sized "pages" and the Physical memory is divided into equal sizes 'frames'. The size of each page is same as that of frame. So one frame of Physical memory holds one page of logical memory. As the logical memory is divided into pages this technique of memory management is called as Paging.

In case of Paging the logical address generated has two parts. The first part contains the page number and the second part contains the offset within the page. The total no. of bits required for logical address depends on the number of Pages and page size.

For e.g. Say Page size is 64 bytes and Program size is 500 bytes. The no. of Pages in logical memory is 8. The logical address bit can be calculated as

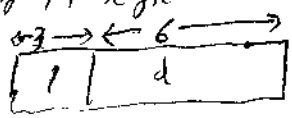
Logical address 

where p – Page no.
d – offset with in Page

No of Pages = 8 Therefore $2^p = 8$ So $p = 3$

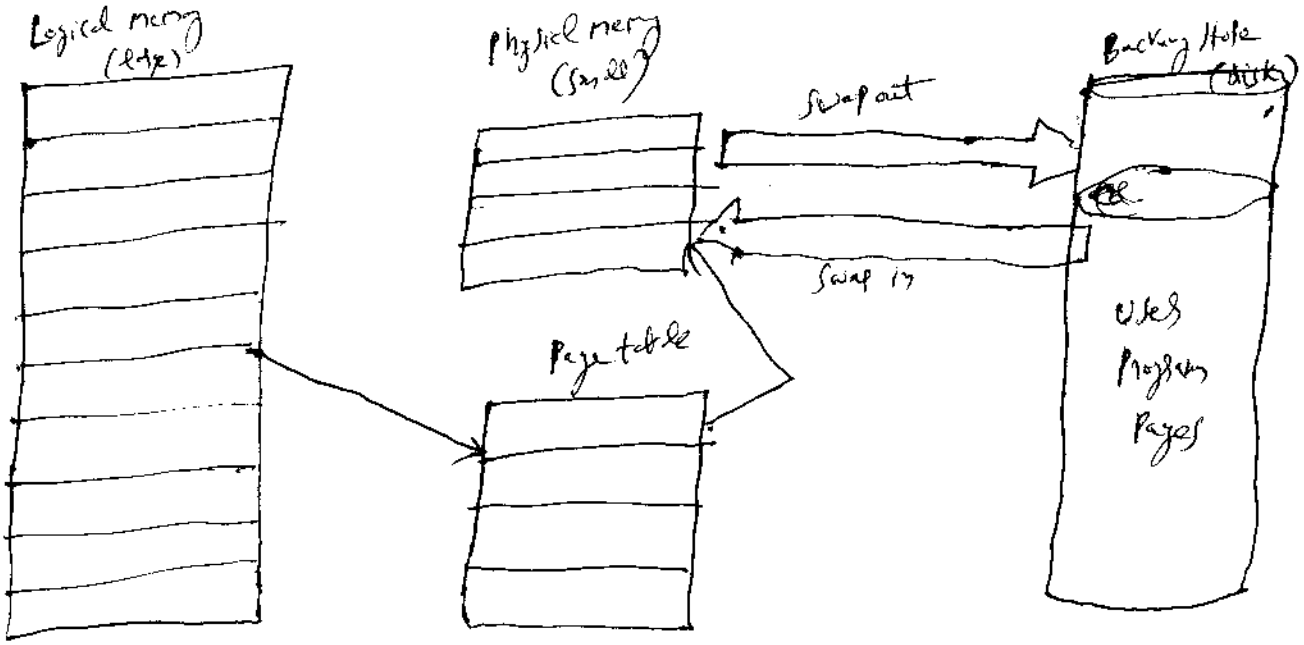
Page size = 64 Therefore $2^d = 64$ So $d = 6$.

Total no of bits in logical address = 3 + 6 = 9



What is virtual memory. Explain with example.

Ans - Virtual memory — Basically the user program that is to be loaded into main memory contains many routines. These all routines may not be executed simultaneously at a time. So there is no need to place the whole program in the beginning itself to start the execution of program. This results in variation of the logical memory and physical memory. So even if the physical memory is small in comparision to the large logical memory it is still possible to execute the program. This concept of memory management is called as virtual memory.



As we see in figure, the logical memory is larger than the physical memory. Initially only the required part of the program is brought into main memory which is large enough to hold that part. Then further required logical memory pages is brought into main memory and if the space is not available, the part of logical memory residing in main memory swapped out and the required page is swapped. So this concept of paging plus swapping is called as virtual memory concept.

Govt. Polytechnic [illegible] Jeedes

Subject :- Basic of Electronics & circuits
(CS-204) (II nd test)

Time :- 12 to 1 PM

Max. Marks - 15

Attempt any three questions
किन्हीं तीन प्रश्नों का उत्तर दीजिये

Q No (1) what is D.C. and A.C. load line. Explain it
D.C. एवं A.C. लोड लाइन को समझाइये ? [5]

Q.No (2) what is operating point ? Explain the factors which affect the bias stability
operating पाइन्ट क्या है ? Bias stability को प्रभावित करने वाले कारकों को समझाइये [5]

QNo (3) Explain the Bias compensation technique using Thermistor and Sensistor [5]
Bias compensation तकनीक को Thermistor एवं sensistor का प्रयोग करते हुए समझाइये ?

QNo (4) Voltage Divider biasing Explain voltage Divider biasing with help of diagram !
Voltage Divider biasing को चित्र द्वारा समझाइये [5]

xxx

CS-204

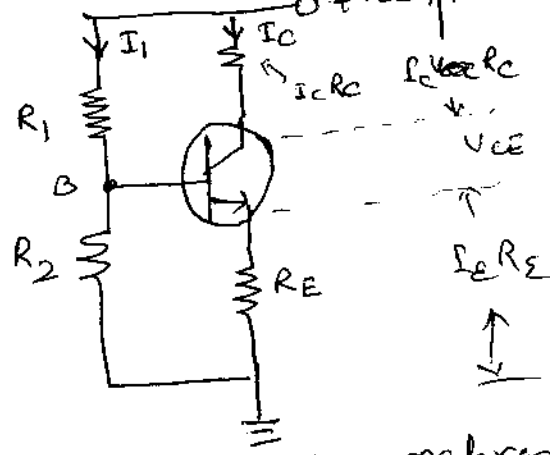
(Basic of Electronic devices & circuits)

IInd test Model paper (Answer)

Q.No. (1) What is A.C. and D.C load line? Explain it

no:→ The relationship between collector-emitter output voltage V_{CE} and collector current I_C is linear and therefore it can be represented by straight line, on the output characteristics giving relation between I_C & V_{CE}. This is known as load line.

* D.C. load line :- The straight line between V_{CE} and I_C when all ~~D~~ a.c. sources to zero and opening all capacitors.



Applying KVL at outer loop

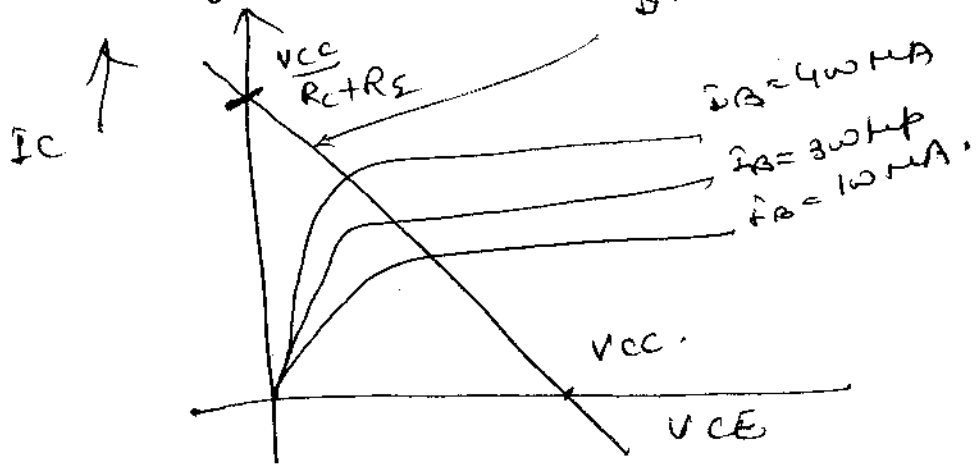
$\Rightarrow V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$\Rightarrow V_{CC} - V_{CE} - I_E R_C - I_C R_E = 0$ $(I_C \simeq I_E)$

$\Rightarrow V_{CC} - V_{CE} = I_C (R_C + R_E)$

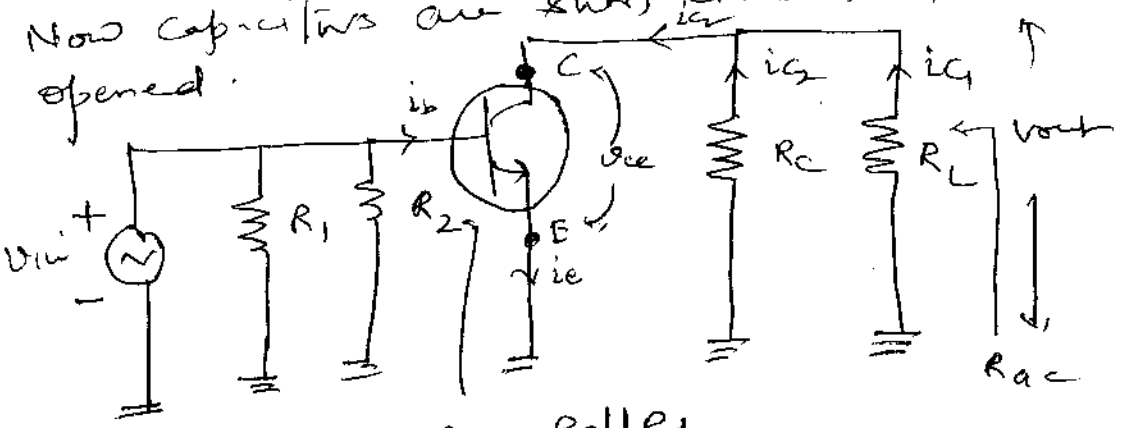
$$\Rightarrow \boxed{I_C = -\frac{V_{CE}}{R_C+R_E} + \frac{V_{CC}}{R_C+R_E}} \quad \text{(1)}$$

eqn (1) can be represented by a straight line at output characteristics.



P.T.O.

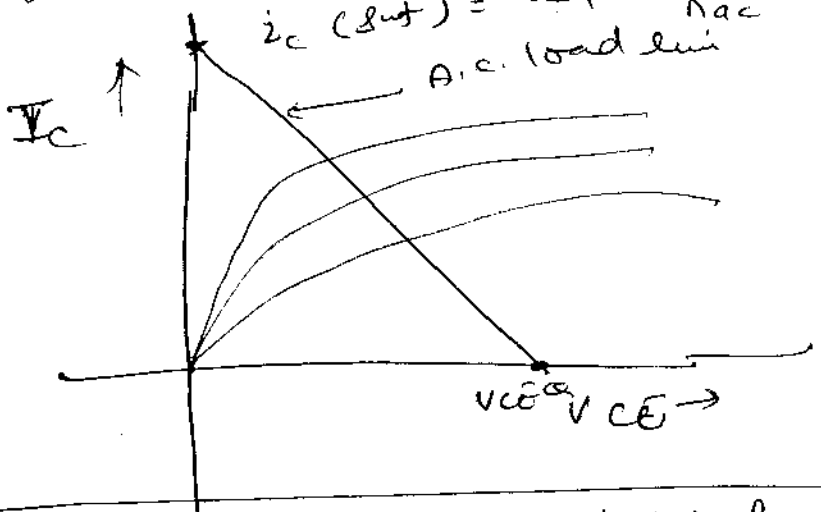
.c. load line :- The straight line at output characteristics when there is input & a.c. signal Now capacitors are short circuited and & d.c are opened. (2)



$R_{AC} = R_C || R_L$

applying KVL and get

$$i_c(sat) = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} \quad \text{—— (1)}$$



Q.No (2) what is operating point & explain the factors which affects the bias stability ?

*Ans :- Q point :- A point on the load line is selected as the dc bias point or quiescent point. This point (bias) specifies the collector current I_C and collector-emitter voltage (V_{CE}) that exist when no input signal is applied.

⇒ factors :- only the fixing of a suitable operating point is not sufficient but it is also to be ensured that the operating point remains stable i.e. it does not shifts due to change in temperature or due to change in transistor parameters.

e stabilization of operating point is essential because of (i) temperature dependence of collector current
(ii) Individual variation
(iii) thermal runaway

(i) Temperature dependance of I_C :-

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

↳ I_{CO} doubles at every 10^0 C.
↳ β increases with temperature
↳ So I_C will increase.

(ii) Individual variation :-

The value of β and V_{BE} are not exactly same for any two transistors even of the same type transistor

(iii) Thermal runaway

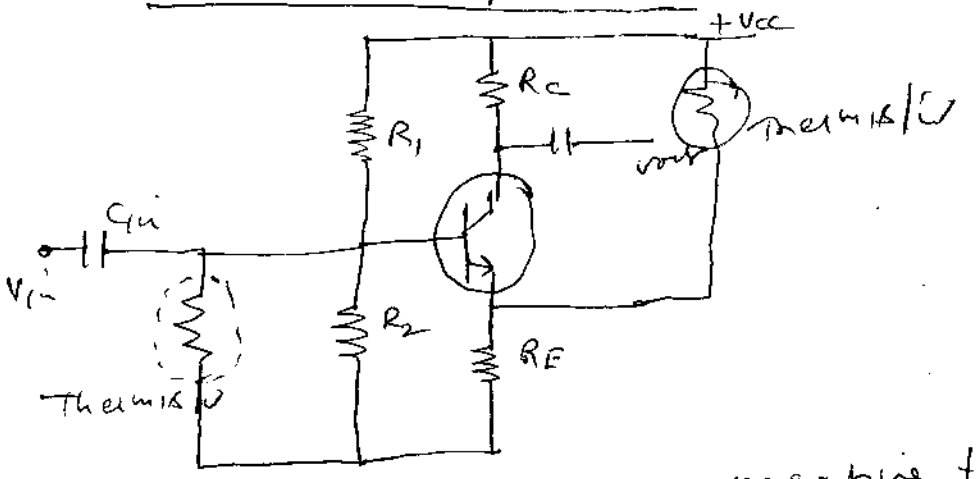
$$I_C = \beta I_B + (1+\beta) I_{CO}$$

when I_C is increased due to β & I_{CO}, which increases the power dissipation, which increases the temperature. Being a cumulative process, it can lead to thermal runaway resulting in burn out of the transistor. The self destruction of an unstabilized transistor is called the thermal runaway.

Q. No (3) Explain the Bias compensation techniques using Thermistor and sensistor.

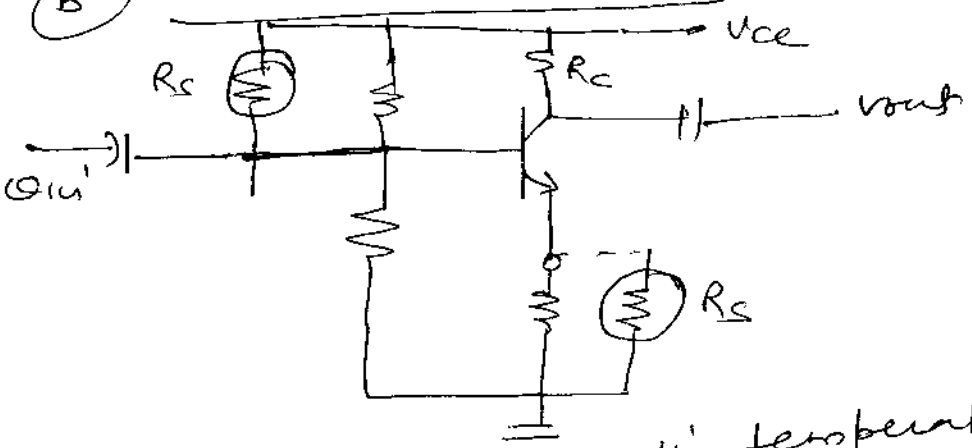
Answer ⇒ Although negative feed back improves the operating point stability but it also reduces the drastically the amplification of the signal. In certain applications the loss in the signal gain may be intolerable and in such cases it is better to use compensating in order to reduce the drift of operating point

Thermistor compensation



The thermistor R_T has a negative temperature coefficient of resistance. The thermistor R_T is used in the circuit to minimize the increase in collector current due to variation in I_{CO}, V_{BE} or β with temperature.

(b) Sensistor compensation

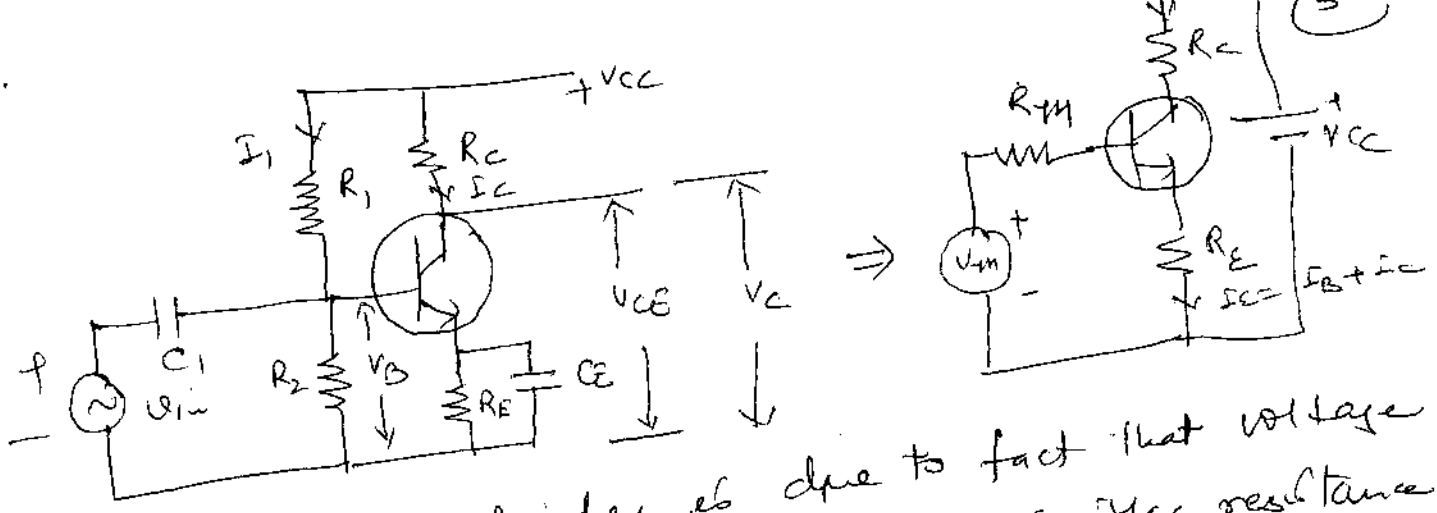


With the increase in temperature, the sensistor resistance of sensistor R_S increases and so the resistance of parallel combination $(R_S // R_1)$. As a result voltage drop across R_2 decreases thereby decreasing the net forward emitter bias.

Q No (4) Explain Voltage Divider biasing with the help of diagram?

Answer: This is most commonly used biasing arrangement. The arrangement shown in figure.

P.T.O.



The name voltage divider is due to fact that voltage divider is formed by R_1 & R_2. The emitter resistance provides stabilization. The resistor R_E causes a voltage drop in direction so as to reverse bias the emitter junction.

$$\text{Here } V_B = \left[\frac{V_{CC}}{R_1+R_2}\right] \cdot R_2$$

$$R_{TH} = R_1 \| R_2 = \frac{R_1 \times R_2}{R_1+R_2}$$

$$V_{TH} = I_B R_{TH} + V_{BE} + I_B \cdot R_E \quad \text{---(1)}$$

$$V_{TH} = I_B R_{TH} + V_{BE} + (I_B + I_C) R_E$$

Diff. w.r.to I_C,

$$0 = R_E + (R_{TH} + R_E)\frac{dI_B}{dI_C}$$

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_{TH}+R_E}$$

$$\boxed{S = \frac{1+\beta}{1+\beta\frac{R_E}{R_{TH}+R_E}}} \quad \text{---(2)}$$

It has low sensitivity to variation in β from one transistor to another of the same lot. It provides better stability than others.

Q1 - डी मार्गन प्रमेय को समझाइए।

Ans) डी मार्गन ने बूलीय बीजगणित के लिए दो महत्वपूर्ण प्रमेय प्रतीपादीत की थी इन दोनो प्रमेय में से एक NAND gate तथा Bubbled OR gate की समतुल्यता की पुष्टि करती है तथा दूसरी प्रमेय NOR gate तथा Bubbled AND gate में समतुल्यता की पुष्टी करती है

- प्रमेय-1 : $\overline{A+B} = \bar{A}.\bar{B}$

प्रमेय-2 : $\overline{A.B} = \bar{A}+\bar{B}$

प्रमेय 1 के अनुसार यदि दो या अधिक चरो के (AND) कम्पलीमेन्ट कर दिया जाये तो यह इन चरो के अलग-अलग कम्पलीमेन्ट का योग (OR) होगा प्रमेय 1 तथा 2 को सिद्ध करने के लिए बीजगणीत $a+\bar{a}=1$ तथा $a.\bar{a}=0$ का प्रयोग करेंगे।

अवरोधन नियमो के अनुसार यदि किसी चरांक को उसके प्रतिलोम के साथ 'OR' किया जाये तो परिणाम सदैव 1 होगा तथा यदि चरांक का उसके प्रतिलोम के साथ गुणन किया जाये तो परिणाम सदैव 0 होगा। यदि पहले नियम को डी मॉर्गन प्रमेय के सदर्भ में लिखा जाय तो $(a+b)+(\bar{a}.\bar{b})$ का मान 1 होना चाहिए।

- बूलीय बीजगणीत के सिद्धान्त अनुसार

$$(A+B)+(\overline{A+B}) = 1 \quad \text{(1)}$$

$$(A+B).(\overline{A+B}) = 0 \quad \text{(2)}$$

इसी (1) समीकरण पर

$$(A+B)+(\overline{A+B}) = 1$$

डी मॉर्गन प्रमेय $\overline{A+B} = \bar{A}.\bar{B}$

$\Rightarrow$ $(A+B)+(\bar{A}.\bar{B})$

$\Rightarrow$ $((A+B)+\bar{A}).((A+B)+\bar{B})$ वितरण नियमानुसार

$\Rightarrow$ $(A+B+\bar{A}).(A+B+\bar{B})$

$(A+\bar{A}+B).(A+B+\bar{B})$ $(A+\bar{A}=1)$

$(1+B).(A+1)$

$(1+A=1)$

$\Rightarrow 1 \cdot 1$

$= 1$

पहला भाग सिद्ध होता है दूसरा भाग $(A+B).(\bar{A}.\bar{B})=0$ को सिद्ध करना है L.H.S. $(A+B).(\bar{A}.\bar{B})$

$\Rightarrow A.\bar{A}.\bar{B} + B.\bar{A}.\bar{B}$ $(A+B=\bar{A}.\bar{B})$ बदलने पर

$\Rightarrow A.\bar{A}\bar{B} + \bar{A}.B.\bar{B}$ $(A.\bar{A}=0)$

$\Rightarrow 0.\bar{B} + \bar{A}.0$

$\Rightarrow 0+0$

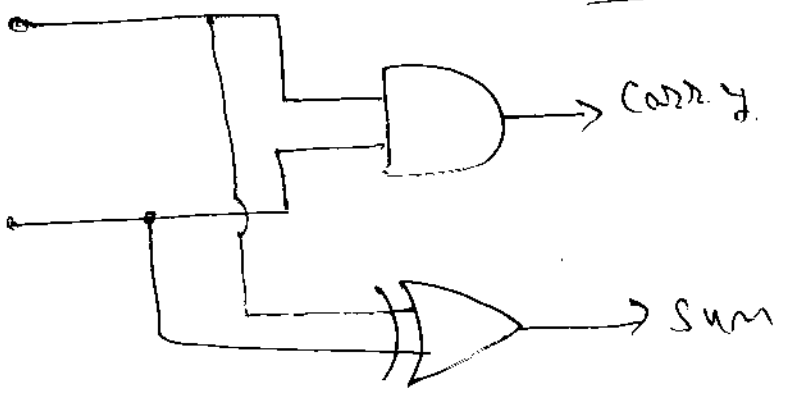
$= 0$

Q.2 बाइनरी Half Adder और Full Adder के बारे में लिखिए।

Ans (1) HALF Adder (अर्द्धयोजक) - बाइनरी संख्याओं का योग निकालने के लिए योजकों का प्रयोग किया जाता है। वह योजक जो मात्र दो बिट्स का योग कर सकता है उसे अर्द्धयोजक कहते हैं इस योजक के दो I/P एवं दो O/P होते हैं I/P के दो बिट होते हैं जिनका मान 0 या 1 हो सकता है O/P में योग (Sum) व हासिल (carry) उत्पन्न होते हैं

Truth table =>

X	y	carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



योग Sum) = $X \oplus Y$

हासिल Carry = $X \cdot Y$.

- Full Adder (पूर्णयोजक) - अर्द्धयोजक जो दो ही बिट का योग निकाल सकता है किन्तु योग करने पर हासिल भी उत्पन्न हो सकती है जिसे अर्द्धयोजक योग में काम में नहीं ले सकता / अतः पूर्ण योजक की आवश्यकता होती है

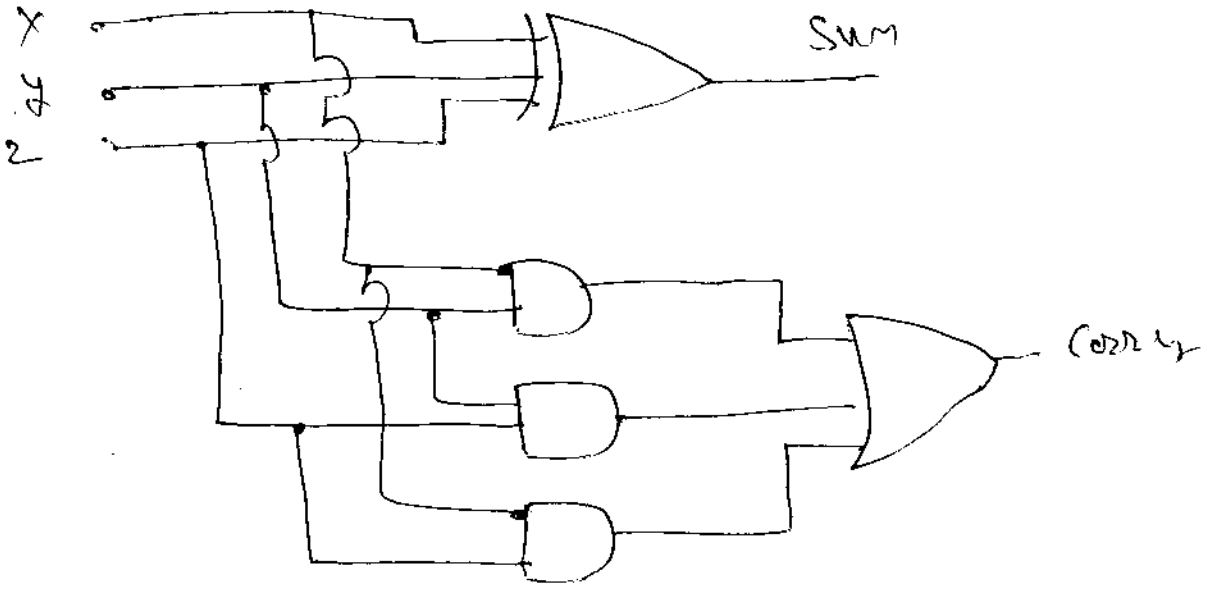
- पूर्णयोजक में तीन I/P संकेत होते है - दो बिट जिनका योग निकालना होता है तथा पिछली बिट के योग से उत्पन्न हासिल।

→ इसकी O/P दो होते है

X	Y	Z	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0

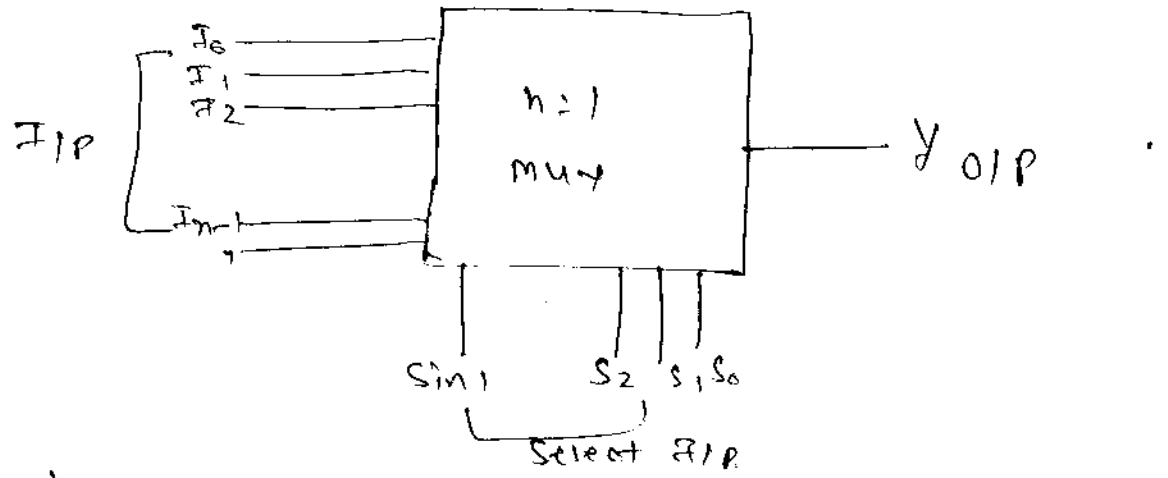
← सत्य सारणी

परिपथ.



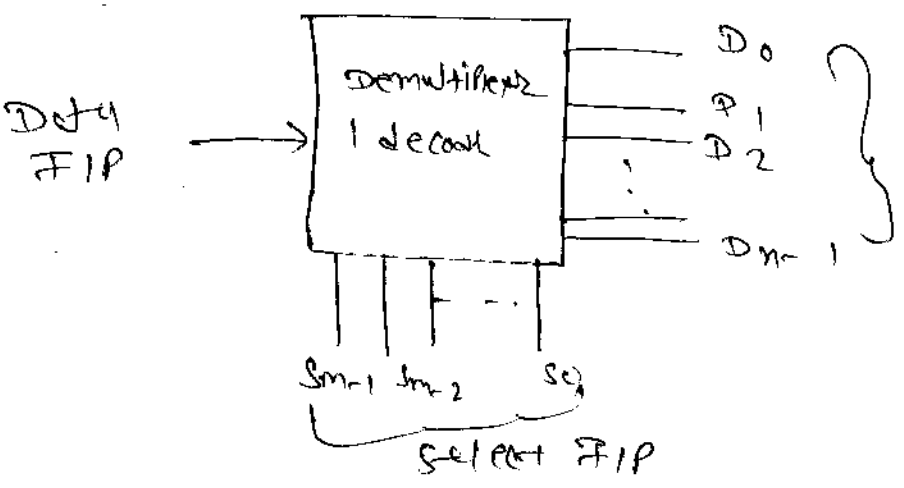
मल्टीप्लेक्सर और डीमल्टीप्लेक्सर के बारे में बताइए।

मल्टीप्लेक्सर - इस नाम से अभिप्राय "अनेक से एक" होता है। मल्टीप्लेक्सर वास्तव में अनेक इनपुट में से केवल एक O/P देता है। मल्टीप्लेक्सर को डिजीटल सर्किटों की संरचनाओं में बहुतायत उपयोग में लाया जाता है।



- इस चित्र में एक n-I/P लाइनों तथा एक O/P लाइन सहित block diagram प्रदर्शित किया गया है। n I/P में से O/P कनेक्शन के लिए एक O/P Select करने के लिए m सलेक्ट I/P के साथ में एक n जगह Source के out को सलेक्ट तथा एक Single out channel को ट्रांसमिट किया जाता है। सामान्यतः multiplexer में प्रायः एक स्ट्रोब लाइन होती है तथा यह सामान्यतः active low होती है जिसका अभिप्राय जब यह निम्न (low) होती है।

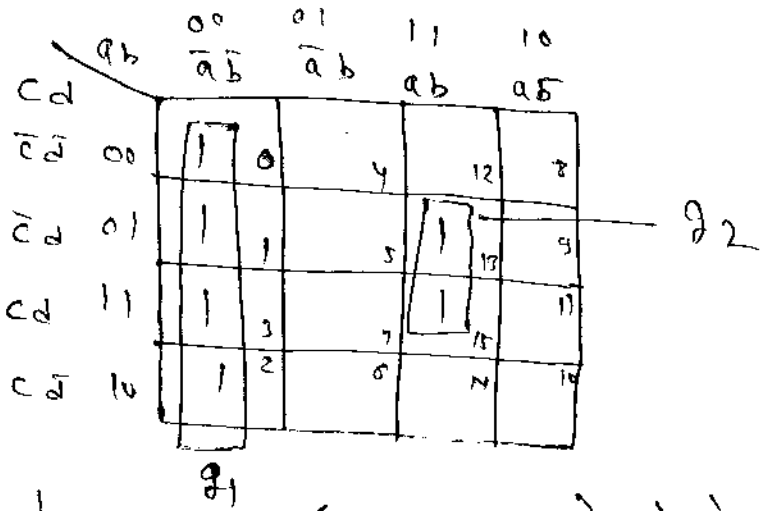
(2) **Demultiplexer** - इसमें केवल 1 इनपुट तथा अनेक आउटपुट लाइनें होती हैं अर्थात एक I/P प्रयुक्त कर उसको एक O/P पर वितरित किया जा सकता है।



In single I/P दिया जाता है तो select line से यह निर्धारित करता कौनसी O/P line से I/P transmit होता है यह सर्किट binary decimal decoder के तरह भी कार्य करता है

सर्किट medium scale integrate (MSI) IC's जिसमें सर्किट codes De multiplexer की सहायता से डिजाइन किया जाता है जब यदि multiple O/P combinational ckt डिजाइन करना हो तब की इसमें न्यूनतम Package Count की आवश्यकता होती है.

Q.4 निम्न फलन $f(a,b,c,d) = \Sigma(0,1,2,3,13,15)$ को K-map की सहायता से सरलीकृत कीजिए।



उक्त फलन के 6 अभिनपद है इन अभिनपदो में से (4) का एक समूह g_1 तथा (g_2) 2 का एक समूह बनाया गया है

$g_1 = m_0 + m_1 + m_2 + m_3$

$= \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}\bar{b}c\bar{d} + \bar{a}bc\bar{d} + a\bar{b}c\bar{d}$

$\Rightarrow a\bar{b}\bar{c}(\bar{d}+d) + \bar{a}\bar{b}c(\bar{d}+d)$

$\Rightarrow \bar{a}\bar{b}\bar{c} + a\bar{b}\bar{c}$ $\quad (d+\bar{d}) = 1$

$\Rightarrow \bar{a}\bar{b}(\bar{c}+c)$

$\Rightarrow \bar{a}\bar{b}$

$g_2 = m_{13} + m_{15}$

$= a\bar{b}c\bar{d} + abcd$ $\quad (c+\bar{c}) = 1$

$\Rightarrow Abd(\bar{c}+c)$

$\Rightarrow abd$

सरलीकरण पश्चात जो फलन हमें मिलता है वह -

$f(a,b,c,d) = a\bar{b} + abd$

Model Paper (Solution) Mid Test

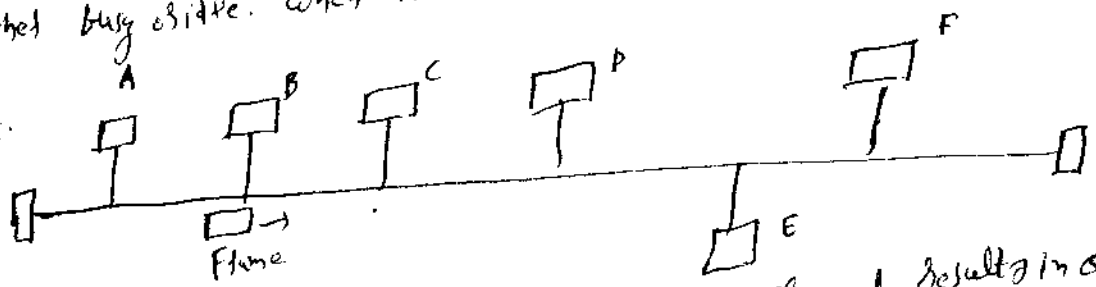
CS-206

Q-1 What is Ethernet. Explain its working.

Ans- The original 802.3 Standard was defined for a Bus-based Co-axial Cable LAN over the bus medium using CSMA/CD for the MAC Protocol. The IEEE 802.3 (CSMA/CD) Standard is generally known as ethernet.

The strategies in which station listen for a carrier and act accordingly are known as Carrier Sense Scheme. The collision can occur only when more than one station begins transmit frame within a short period.

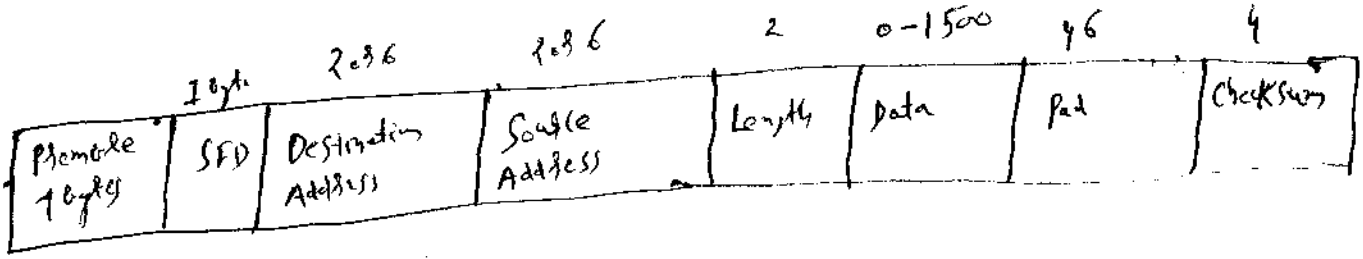
In this scheme a station that wishes to transmit first listen to channel to see it transmit. State either busy or idle. When the channel is sensed to be idle, the station can



For eg if the two stations starts transmitting simultaneously and results in a collision. Then all transmissions are stopped and sends a Jamming signal to all the stations of this collision.

Ethernet Frame Structure-

Fig shows the frame format for the IEEE 802.3 LAN Protocol



rat are the various services provided by data link layer

The Basic Purpose of data link layers is to provide service to network layer, establish, maintain and release data link connection between stations using one of more physical lines, it also deals with transmission errors, error control, flow control and link management issue between transmitter and receiver.

The various services provided by data link layer are

(1) Error Control - Since some errors introduce during transmission are inevitable. The data link layer protocol contains some error control capability to detect and correct errors to maintain high degree of Integrity.

(2) Data Synchronization - For the receiver to correctly find out boundary of the message that has arrived, a framing technique for acquiring and maintaining synchronization between the transmitter and receiver is used.

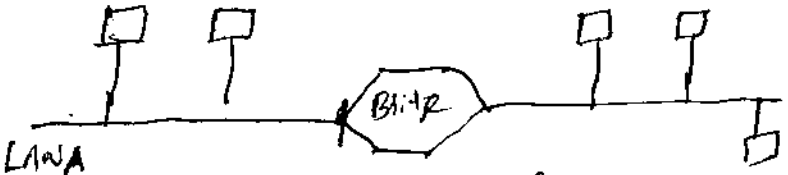
(3) Flow Control - This is a technique for ensuring that sender does not overwhelm a receiver with data.

(4) Link management - The initiation, maintenance, and termination of the data link requires a proper coordination and co-operation among the stations. The link termination does not necessarily mean that the physical path is disconnected.

Explain the following

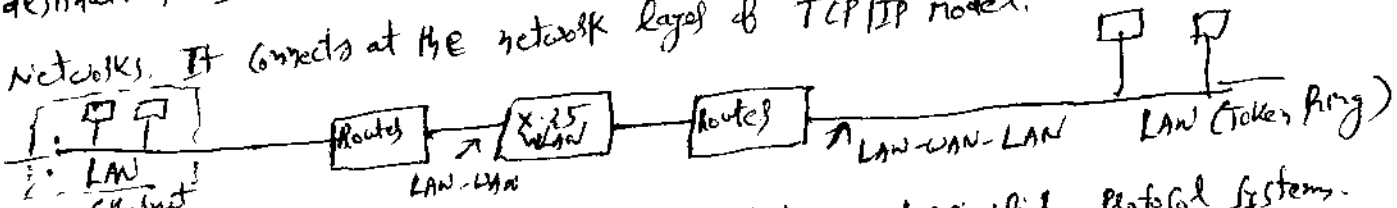
i) Routers ii) Bridges iii) Gateways

Bridge :- Bridge can extend the maximum size of network. Bridge can connect network with dissimilar data frames. For eg Bridge can connect Token Ring LAN to Token BUS LAN.

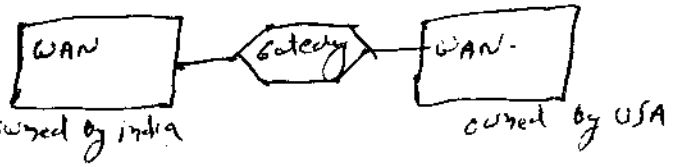


The Bridge working is shown in fig. The Bridge receives every Packet on LAN A and LAN B. Packets on LAN A, address to destination on LAN B, are retransmitted to LAN B for delivery. Similar actions for Packet on LAN B are retransmitted to LAN A. Rest of the Packets are discarded.

Routers - When multiple routes exist in large networks, where some routes are considerably slower than others. Routers handle such traffic. Routers uses the routing algorithm to determine the most efficient route for sending a Packet over a network to the destination. It is an internetwork connecting device. It connects two heterogeneous networks. It connects at the network layer of TCP/IP model.



Gateways - Gateways enable communication between dissimilar Protocol systems. The functioning of gateway depends on the Protocol translation, which it must perform. The gateways commonly functions at the Application layer of the TCP/IP model.



Gateway connect dissimilar environment by removing layered Protocol.

Explain Stop and wait Protocol.

Ans. 1 bit Stop-and-wait Sliding window Protocol -

In this Protocol the Sender's and Receiver's window buffers size is 1-bit, that means it can transmit/receive frames sequence of 1 at a time. Such a Protocol uses Stop-and-wait ARQ system.

Since the Sender transmits a frame and wait for its acknowledgement before sending the next one.

The problem with this Protocol is that only one frame at a time can be transmit. It support full duplex transmission. For eg that Machine A is trying to send its frame(1) to Machine B and B is trying to send its frame (1) to A. Both Machine acknowledged frame while transmitting their frame.

Govt. Polytechnic College [illegible]

Subject :- Microprocessor & Interfacing (CS-208)
(End Test)

Max. Marks 15 Time 12.00 PM to 1.00

Attempt any three questions.

(1) Explain following instructions
(a) MOV r_1, r_2 (c) STAX rp (e) ~~ADDr~~ ADD r
(b) LDA addr (d) LHLD addr.
[1×5 = 5]

(2) Explain following instructions
(a) DAD rp (c) DCR r (e) ORA m
(b) SUB m (d) ANA r [1×5 = 5]

(3) Explain different types of interrupts of 8085 with examples [5]

(4) Explain different addressing modes of 8085 [5]

XX

IInd test

Model answer

Sub:- Microprocessor and Interfacing (cs-208)

Q.No (1) Explain following instructions

Ans:- (a) MOV R_1, R_2

* It is a 1-byte instruction
* copies data from source register R_2 to destination register R_1

(b) STAX RP

* copy or store of data (A → Accumulator) into memory indicated by the register pair

(c) LDA addr

* copy (M → memory data) into Accumulator. memory specified by the 16 bit address.

(d) LHDL addr

This instruction loads the contents of 16 bit memory location into the HL Pair.

(e) Addr

The data of memory (M) added to ACCumulator.

Q.No. (2) Explain following instruction

Ans:- (a) DAD RP →

- Add register pair contents to HL Pair

(b) DCR R →

- This is 1 byte instruction
- Decreases the contents of register R by 1

SUB M

- This is 1-byte instruction
- Subtracts the contents of Reg memory and store the result in ~~accumulator~~ accumulator.

(d) ANA R

- This is 1-byte instruction
- Logically ANDs the contents of the Register R with contents of the accumulator.

(e) ORA M

- This is 1 byte instruction
- logically ORs the content of Memory with the contents of accumulator.

Q No (3) Explain different type of interrupts of 8085 with examples.

Answer → The Intel 8085 has five interrupts inputs namely TRP, RST 7.5, RST 6.5, RST 5.5, INTR. The TRAP has the highest priority followed by RST 7.5, RST 6.5, RST 5.5, INTR. The INTR has the lowest priority. When interrupts are to be used they are enabled by software using instruction (EI) in the main program. The instruction EI sets the interrupt enable flip flop to enable the interrupts. The instruction DI (Disable Interrupt) is used to disable interrupt.

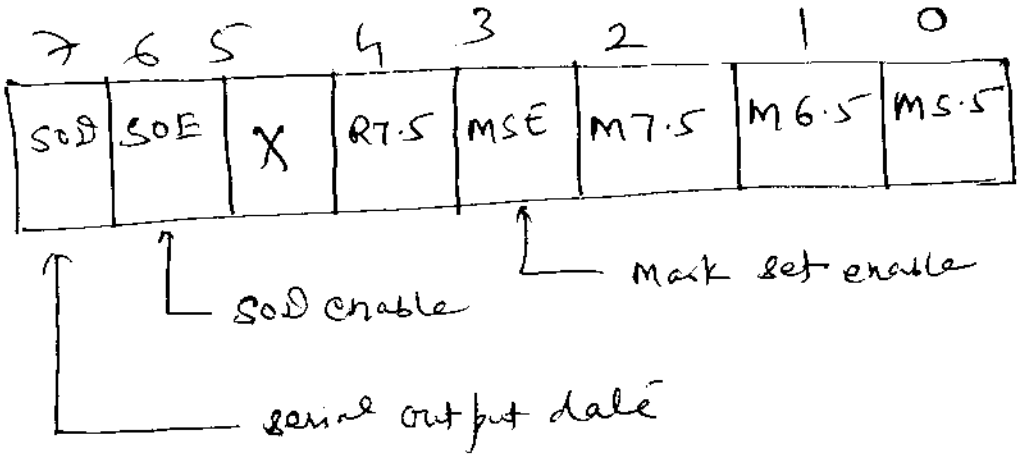
When an interrupt line goes to high the processor complete its current instruction and saves program counter on the stack.

Hardware & Software Interrupts :- Interrupts caused by devices are called hardware interrupt. The normal operation of microprocessor can be interrupted by special instructions. Such an interrupt is called software interrupt.

Interrupt	Call location in Hex
TRP	0024
RST 7.5	003C
RST 6.5	0034
RST 5.5	002C

* Vectored interrupt :- An interrupt for which hardware automatically transfers the program to a specific memory location is known as vectored interrupt.

* RST 7.5, 6.5 and 5.5 :- These are maskable interrupt. These interrupts are enabled by EI & SIM.



Diag:- ~~Accumulator~~ Accumulator content for SIM

(4)

Explain different addressing modes of 8085

Each instruction requires certain data on which it has to operate. It has already seen explained that there are various techniques to specify data for instructions. These techniques are called addressing modes. Intel 8085 uses the following addressing modes.

1. Direct addressing
2. Register addressing
3. Register indirect addressing
4. Immediate addressing
5. Implicit Addressing

Direct addressing :- In this mode of addressing the address of the operand (data) is given in instruction itself.

Example (A) STA 240H

02, 00, 24

(B) IN 02

DB, 02

(C) Register addressing :- In register addressing mode the operands are in the general purpose register. The opcode specifies the address of the registers in addition to the operation of to be performed

(a) MOV A, B

78

(b) Add B

80

P.T.O.

ster Indirect Addressing

, this mode of addressing the address of operand is specified by a register pair.

(a) LXI H, 2500H
MOV A, M
HLT

(b) LXI H, 2500H
~~ADD~~ M
HLT

Immediate Addressing :- In this operand is specified within instruction itself. examples are

(a) MVI A, 05
3E, 05

(b) ADI 06
C6, 06

Implicit Addressing

These are certain instruction which operate on the content of the accumulator. Such instruction do not require the address of the operand. examples are

↳ CMA
↳ RAL
↳ RAR

xx

CS-210

Q-1 Explain the process of installation of CD-Rom drive.

Ans- To Add an internal IDE CD-Rom drive following steps are used.

1. Open the CPU
2. Check for an available 4 Pin Power Connector.
3. Attach the 4 Pin Power Connector to the drive
4. Mount the new drive into the 5¼" expansion bay.
5. Attach the Cable (40 Pin) noting the key in Connector.
6. Connect the audio Cable supplied with the CD drive to the Sound Card.
7. Using Installation floppy disk supplied with CD drive run Setup to Copy necessary driver files.
8. Reboot the System.

Q-2 Explain the following
i) Serial Port ii) Parallel Port iii) USB Port

Serial Port — It is a 9 Pin and 25 Pin port having male type of connector on Computer side. It is used to connect external modems and older Computer mouse. In Mark Ports data travels at 115 Kb/Sec

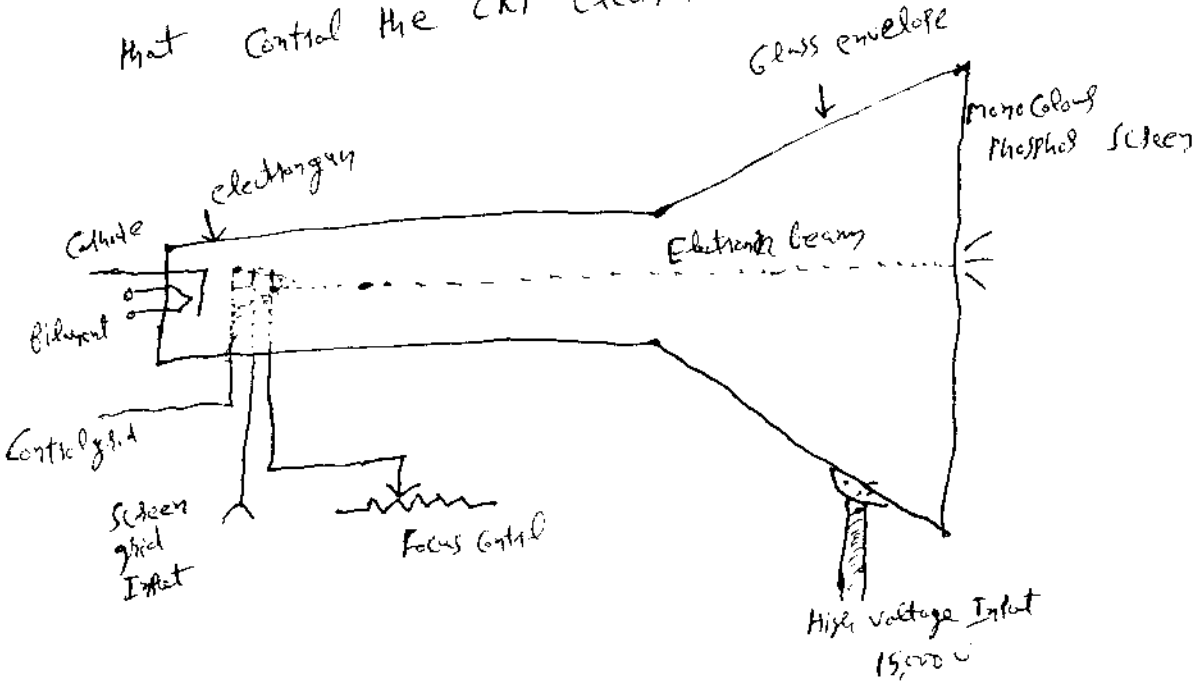
Parallel Port — It has 9 Pin and 25 Pin Connector of Female type on the Computer side. It is used to connect printers. It is also called as printer Port.

Post – Universal Serial Bus Port

This port can connect all kinds of external USB devices such as external hard disk, Printers, Scanners, Mouse etc. In these ports data travel at 12 megabits/sec. USB Compliant devices can get power from a USB port.

Q-3 Explain the Concept of CRT with diagram.

Ans. A Computer monitor contains a Cathode Ray tube (CRT) and some electronics that control the CRT electron Beam and a Power Supply.



The Principle of operation of CRT is shown in fig. The CRT is a evacuated glass tube. It has a Phosphor coating on the inside of the large screen and an electron gun at the narrow end. The gun fires a narrow beam of electrons at the screen. When beam hits the Phosphor Coating, light is given off.

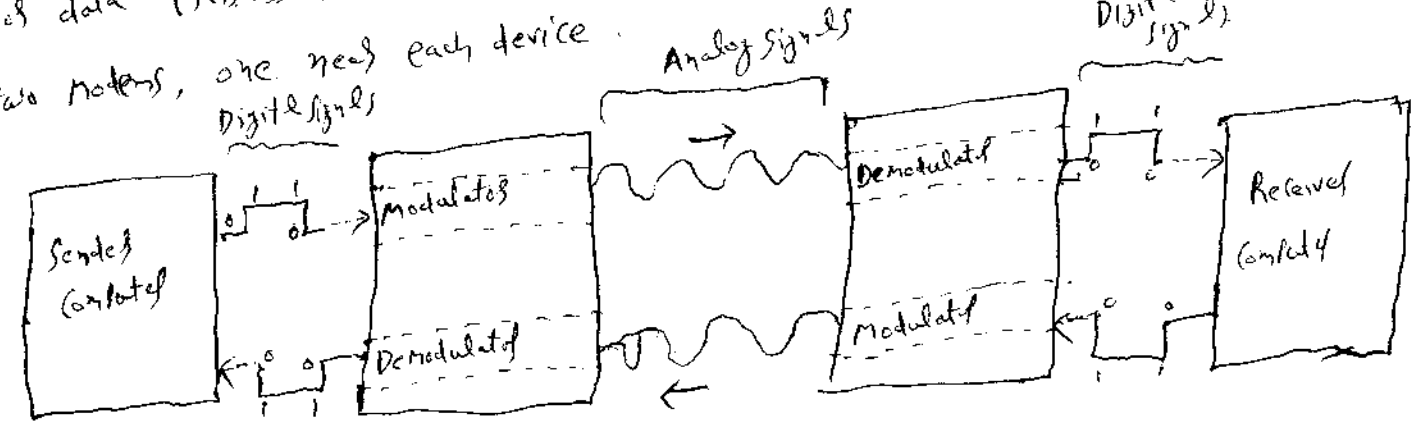
Explain the following

i) Scanner ii) Modem.

Scanner - Scanner is an input device which captures image and sends digital information to the computer.

Scanner is an optical device used to digitize images such as line art of photographs of even text. This digital information after image capturing can be edited or manipulated using desktop publishing softwares to get a quality output of the image. Text can also be merged with the graphics scanned easily. A light source illuminates the image. Black or white spaces reflects more light than coloured or inked letter or images. Either the image or scan head is moved from one side to another to capture the bounced off light from the image. The reflected image is routed through series of mirrors to lens after passing through colour filters. The lens focuses the beam of light onto a photo sensitive charge coupled device sensor strip with 1024 elements. Each element samples the light sensitivity that corresponds to a spot on the image. Each element can detect 256 different light levels.

Modem - Modem is basically Modulator/Demodulator to perform modulation and demodulation. Hence when a data communication system uses an analog facility for data transmission between two digital devices (i.e. two computers), it requires two modems, one near each device.



shown in fig when the sender's computer generate and sends digital signal, data's & the modem placed near sender's computer converts it to analog form. The communication system then transmits this analog signal through telephone lines up to the modem near the receiver's computer's. The demodulator of this modem then converts analog signal to digital signal form and passes on the digital data to receiver's computer's.