Government of Rajasthan

GOVERNMENT POLYTECHNIC COLLEGE, PALI

Year: 3rd yr **Branch: Electronics** **Session: 2017-18**

EL-307: Linear Integrated Circuit & Design

III MID TERM TEST

Duration: 1 Hr. **Max. Marks: 15**

Note: *Attempt any THREE questions. All question carry equal marks.*

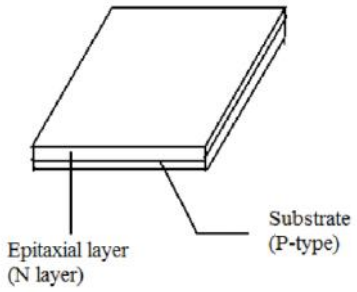
Q.1 Explain the steps to manufacture monolithic transistor.

मोनोलिथिक ट्रांजिस्टर बनाने के चरणों को समझाइये!

Ans.) The fabrication of a monolithic transistor includes the following steps. 1. Epitaxial growth 2. Oxidation 3. Photolithography 4. Isolation diffusion 5. Base diffusion 6. Emitter diffusion 7. Contact mask 8. Aluminium metallization 9. Passivation

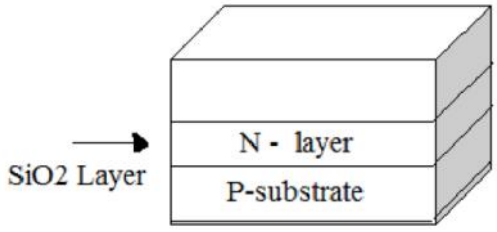
The letters P and N in the figures refer to type of doping, and a minus (-) or plus (+) with P and N indicates lighter or heavier doping respectively.

1. **Epitaxial growth:** The first step in transistor fabrication is creation of the collector region. We normally require a low resistivity path for the collector current.



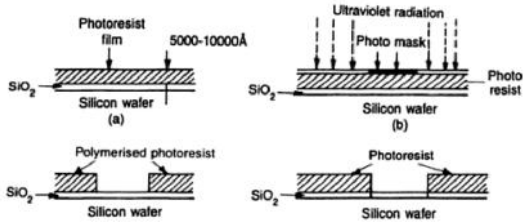
Then, an epitaxial layer of lightly doped N-silicon is grown on the P-type substrate by placing the wafer in the furnace at 12000 C and introducing a gas containing phosphorus (donor impurity). The resulting structure is shown in figure

2. **Oxidation:** As shown in figure, a thin layer of silicon dioxide (SiO2) is grown over the N-type layer by exposing the silicon wafer to an oxygen atmosphere at about 10000 C.



3. **Photolithography:** The prime use of photolithography in IC manufacturing is to selectively etch or remove the SiO2 layer. As shown in figure, the surface of the oxide is first covered with a thin uniform layer of photosensitive emulsion (Photo resist). The mask, a black and white negative of the required pattern, is placed over the structure. When exposed to ultraviolet light, the photo

resist under the transparent region of the mask becomes poly-merized. The mask is then removed and the wafer is treated chemically that removes the unexposed portions of the photo resist film. The polymerized region is cured so that it becomes resistant to corrosion. Then the chip is dipped in an etching solution of hydrofluoric acid which removes the oxide layer not protected by the polymerized photo resist. This creates openings in the SiO2 layer through which P-type or N-type impurities can be diffused using the isolation diffusion process as shown in figure. After diffusion of impurities, the polymerized photo resist is removed with sulphuric acid and by a mechanical abrasion process.



4. **Isolation Diffusion:** Since a number of devices are to be fabricated on the same IC chip, it becomes necessary to provide good isolation between various components and their interconnections.

   In PN junction isolation technique, the P+ type impurities are selectively diffused into the N-type epitaxial layer so that it touches the P-type substrate at the bottom. This method generated N-type isolation regions surrounded by P-type moats. If the P-substrate is held at the most negative potential, the diodes will become reverse-biased, thus providing isolation between these islands.

5. **Base diffusion:** For NPN transistor, the base is diffused in a furnace using a boron source. The diffusion process is done in two steps, pre deposition of dopants at 9000 C and driving them in at about 12000 C. The drive-in is done in an oxidizing ambience, so that oxide is grown over the base region for subsequent fabrication steps.

6. **Emitter Diffusion:** Emitter Diffusion is the final step in the fabrication of the transistor. The emitter opening must lie wholly within the base. The emitter diffusion is normally a heavy N-type diffusion, producing low-resistivity layer that can inject charge easily into the base. A Phosphorus source is commonly used.

7. **Contact Mask:** After the fabrication of emitter, windows are etched into the N-type regions where contacts are to be made for collector and emitter terminals. Heavily concentrated phosphorus N+ dopant is diffused into these regions simultaneously.

8. **Metallization:** The IC chip is now complete with the active and passive devices, and the metal leads are to be formed for making connections with the terminals of the devices. Aluminium is deposited over the entire wafer by vacuum deposition. Metallization is carried out by evaporating aluminium over the entire surface and then selectively etching away aluminium to leave behind the desired interconnection and bonding pads.

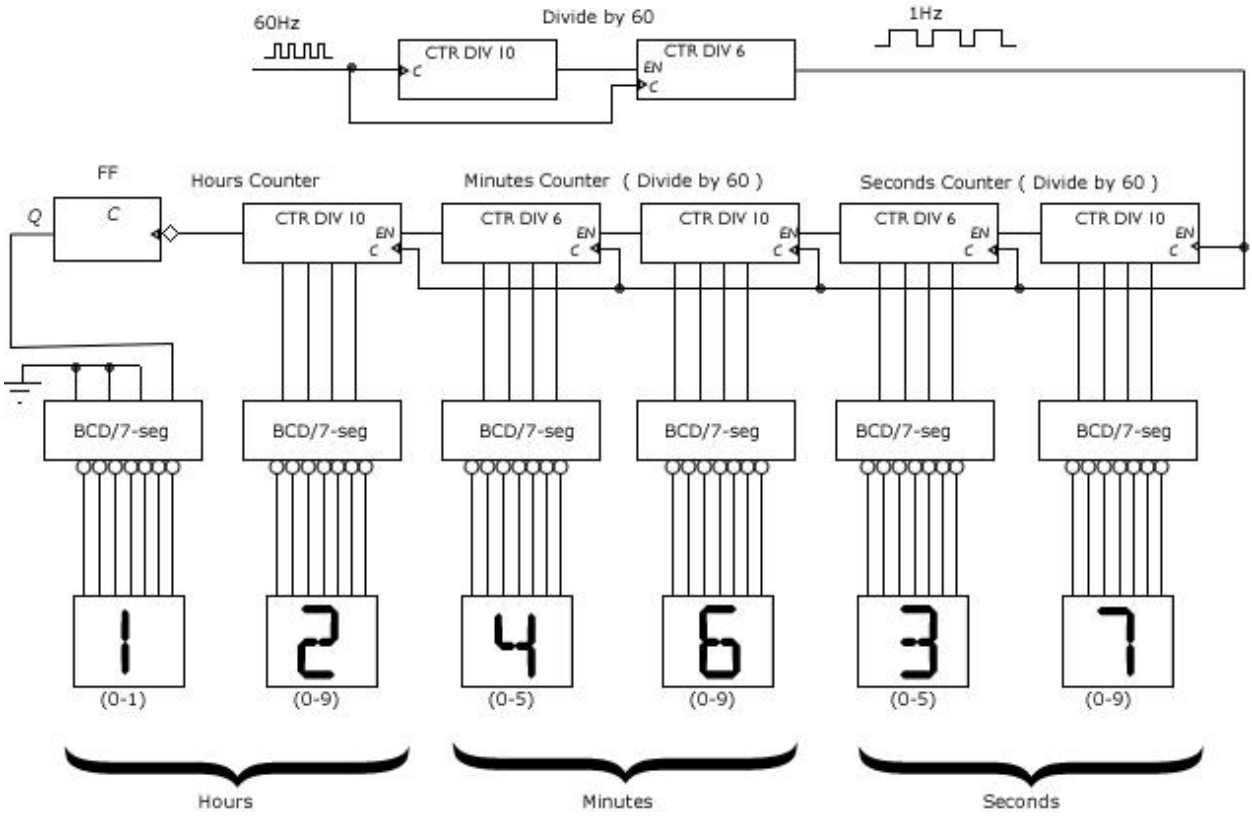
9. **Passivation/ Assembly and Packaging:** Metallization is followed by passivation, in which an insulating and protective layer is deposited over the whole device. This protects it against mechanical and chemical damage during subsequent processing steps

Q.2 Design digital clock.

डिजिटल क्लॉक डिजाईन करिए

Ans.) The 4 blocks of a digital clock are

- 1 Hz clock generator to generate 1 PPS (pulse per second) signal to the seconds block.
- SECONDS block - contains a divide by 10 circuit followed by a divide by 6 circuit. Will generate a 1 PPM (pulse per minute) signal to the minutes block. The BCD outputs connect to the BCD to Seven Segment circuit to display the seconds values.
- MINUTES block - identical to the seconds block it contains 2 dividers; a divide by 10 followed by a divide by 6. Will generate a 1 PPH (pulse per hour) signal to the HOURS block. The BCD outputs connects to the BCD to Seven Segment circuit to display the minutes values.
- HOURS block - depending on whether it is a 12 or 24H clock, will have a divide 24 or divide by 12. For 24H, it will count from 00 to 23. For 12H, it will count from 00 to 11. The BCD outputs connects to the BCD to Seven Segment circuit to display the hours values.



Q.3 Design 2 bit simultaneous analog to digital converter.

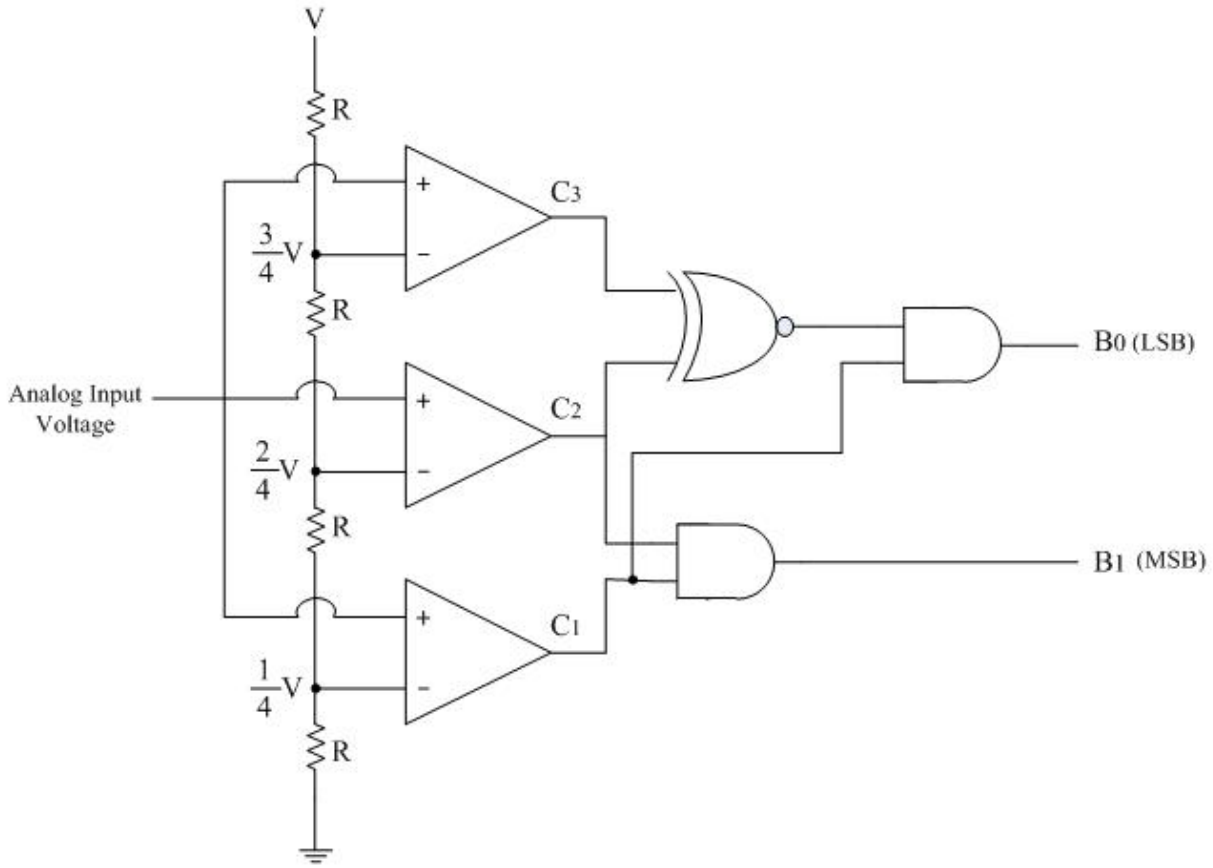
2-बिट simultaneous एनालॉग टू डिजिटल कनवटर डिजाईन करिए

Ans.) Flash Type ADC is based on the principle of comparing analog input voltage with a set of reference voltages.

To convert the analog input voltage into a digital signal of n-bit output, (2n – 1) comparators

are required.

The following figure shows 2- bit flash type ADC



The three op-amps are used as comparators. The non-inverting inputs of all the three comparators are connected to the analog input voltage. The inverting terminals are connected to a set of reference voltages (V/4), (2V/4) and (3V/4) respectively which are obtained using a resistive divider network and power supply +V.

The output of the comparator is in positive saturation(i.e. logic 1), when voltage at non-inverting terminal is greater than voltage at inverting terminal and is in negative saturation otherwise.

The following table shows the comparator outputs for different ranges of analog input voltages and their corresponding digital outputs.

Analog Input Conditions	Comparator Outputs			Digital output	
	C_1	C_2	C_3	B_1	B_0
$0 \leqslant V_{in} \leqslant \frac{V}{4}$	0	0	0	0	0
$\frac{V}{4} \leqslant V_{in} \leqslant \frac{2V}{4}$	1	0	0	0	1
$\frac{2V}{4} \leqslant V_{in} \leqslant \frac{3V}{4}$	1	1	0	1	0
$\frac{3V}{4} \leqslant V_{in} \leqslant V$	1	1	1	1	1

Consider first condition, where analog input voltage VA is less than (V/4). In this case, the voltage at the non-inverting terminals of all the three comparators is less than the respective voltages at inverting terminals and hence the comparator outputs are C1C2C3 = 000. This comparator outputs are applied to the further coding circuit to get the digital outputs as B1B0 = 00

Similarly the digital outputs are calculated for other three conditions also.

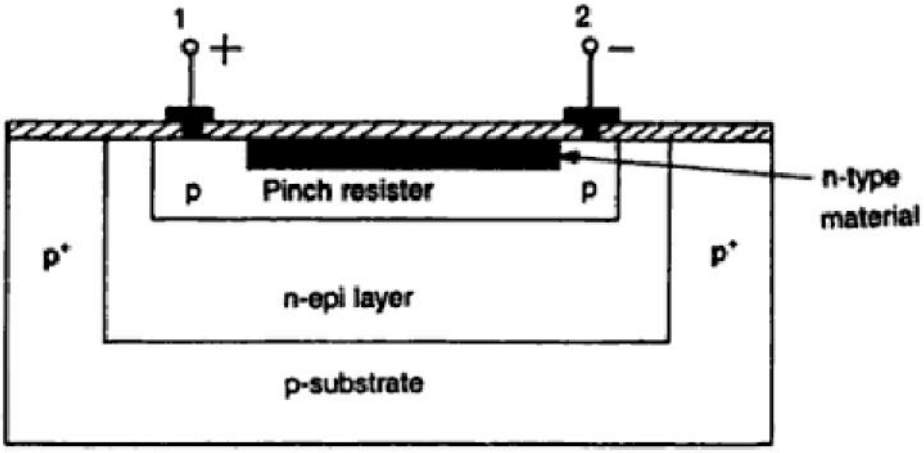
Q.4 Write short note on integrated resistor.

इंटीग्रेटेड रजिस्टर पर लघु टिपण्णी लिखिए !

Ans.) A resistor in a monolithic integrated circuit is obtained by utilizing the bulk resistivity of the diffused volume of semiconductor region. The commonly used methods for fabricating integrated resistors are 1. Diffused 2. epitaxial 3. Pinched and 4. Thin film techniques.

Pinched resistor

The sheet resistance offered by the diffusion regions can be increased by narrowing down its cross-sectional area. This type of resistance is normally achieved in the base region. Figure shows a pinched base diffused resistor. It can offer resistance of the order of mega ohms in a comparatively smaller area. In the structure shown, no current can flow in the N-type material since the diode realized at contact 2 is biased in reversed direction. Only very small reverse saturation current can flow in conduction path for the current has been reduced or pinched. Therefore, the resistance between the contact 1 and 2 increases as the width narrows down and hence it acts as a pinched resistor.



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